ABSTRACT OF THE DISCLOSURE

An image processor has a controller unit connected to at least one of functional units such as an image reading unit, detects a source of input of image data according to a network I/F or a parallel bus I/F. An image-memory access control section transmits the image data input from each of the functional units to a memory group and also transmits the image data stored in the memory group to the functional unit. A system controller controls the overall apparatus and also controls the image-memory access control section according to the input source of the image data to determine an order of transmitting the image data to the memory group.